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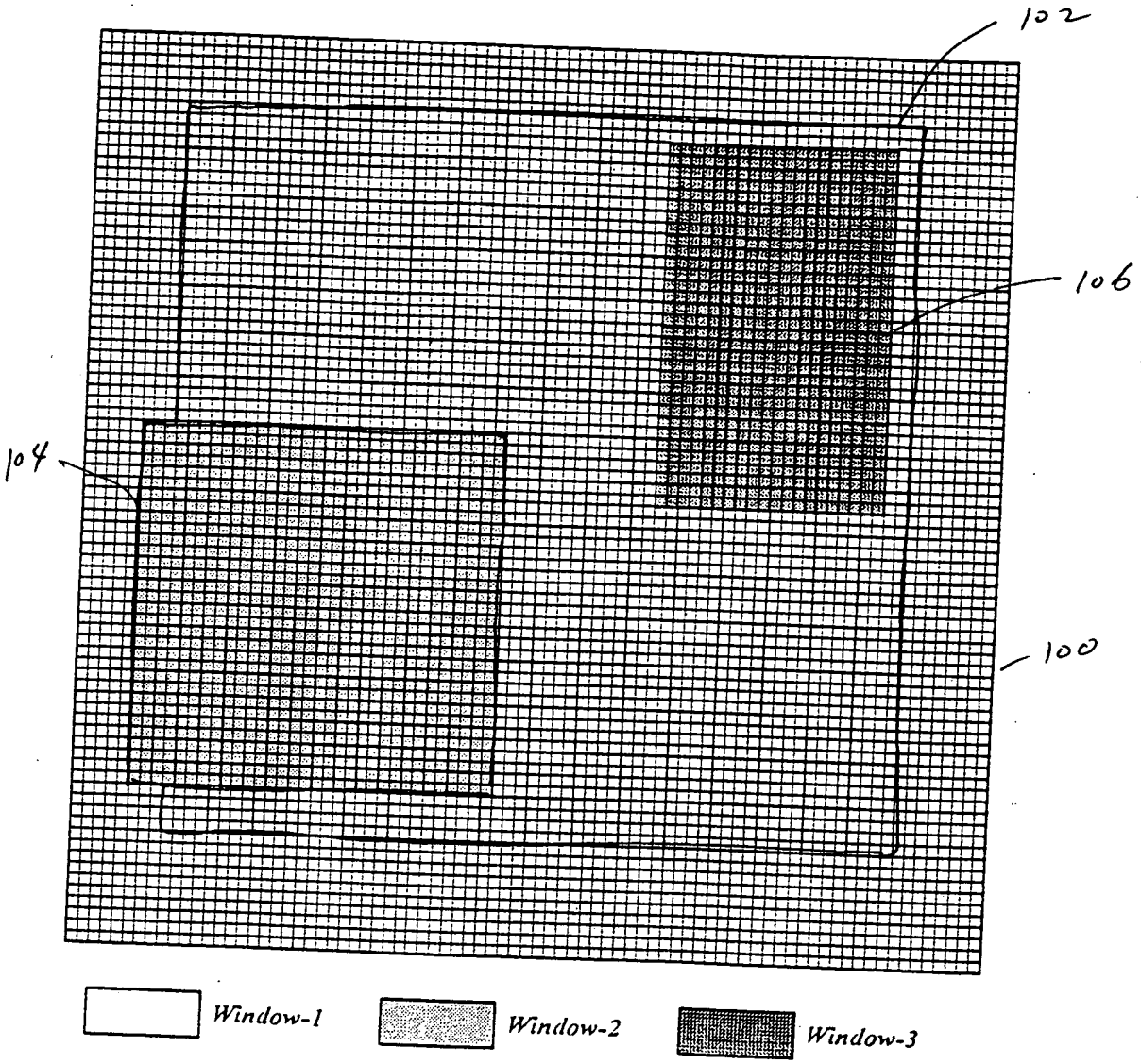


Figure 1A *Window configuration of first foveal vision APS chip.*

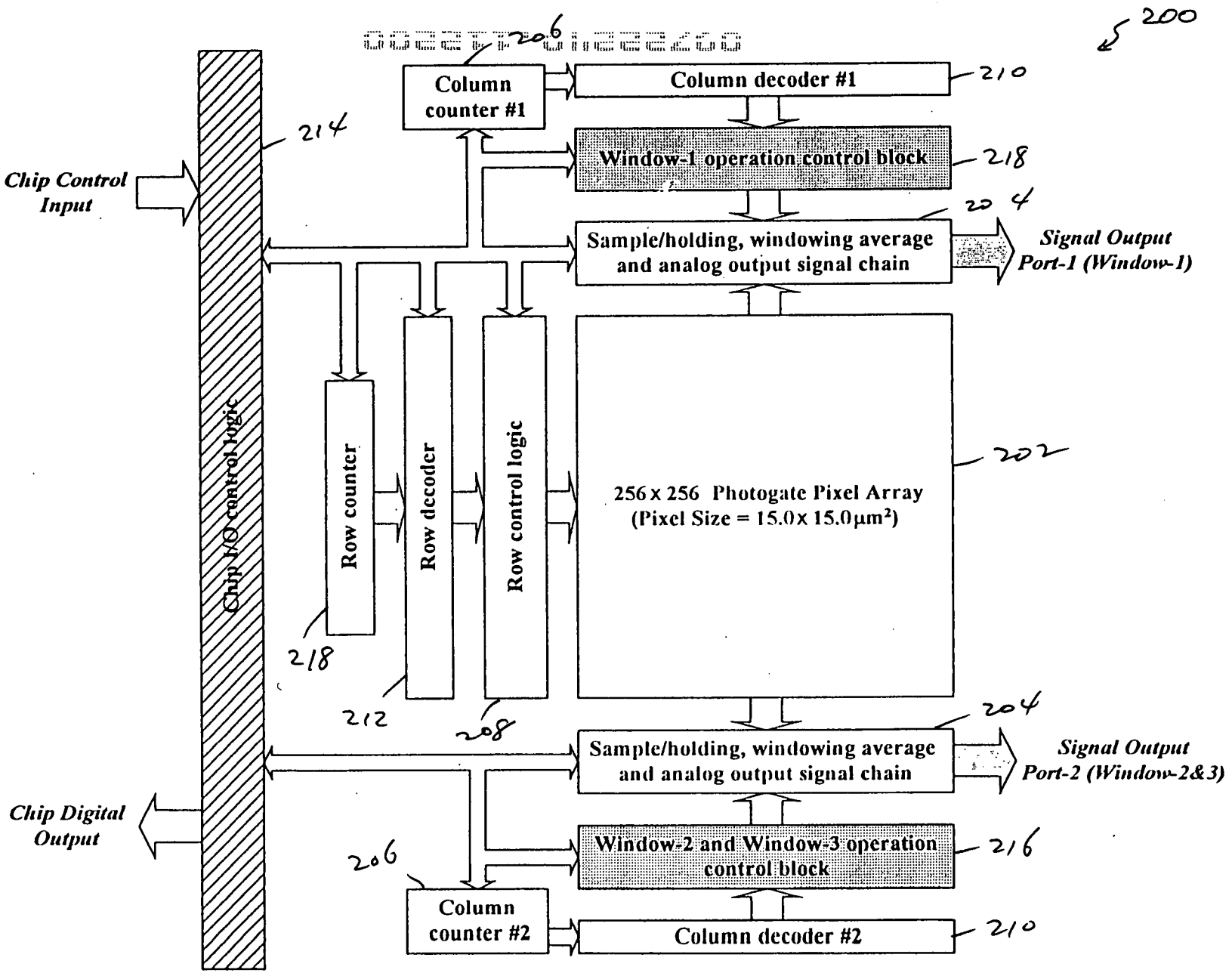


Figure 2A *Foveal vision APS chip design architecture.*

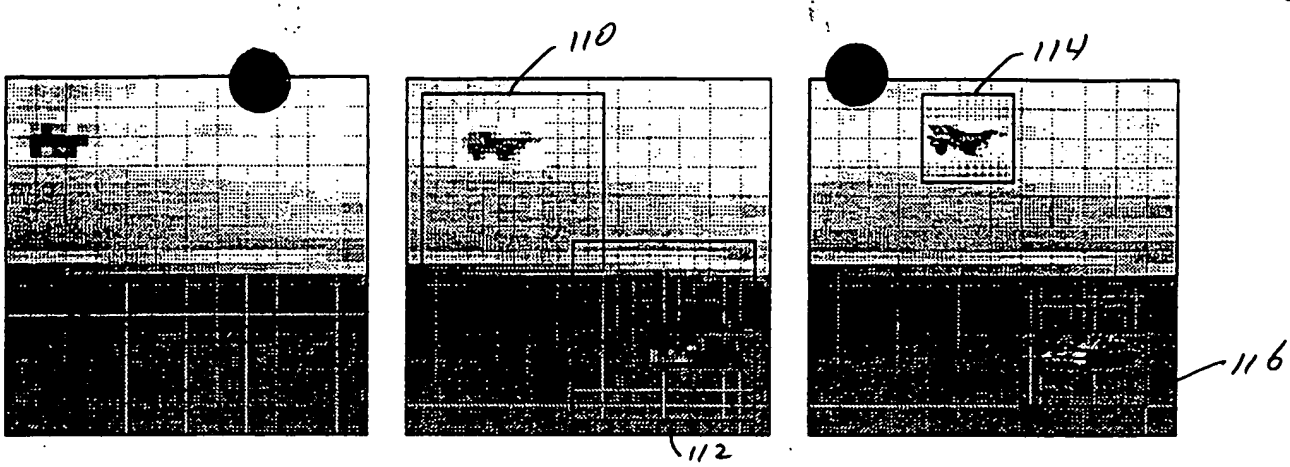


Figure 1B Evolution of the topology of the dynamically reconfigurable imager that combines wide FOV searching with high-resolution tracking

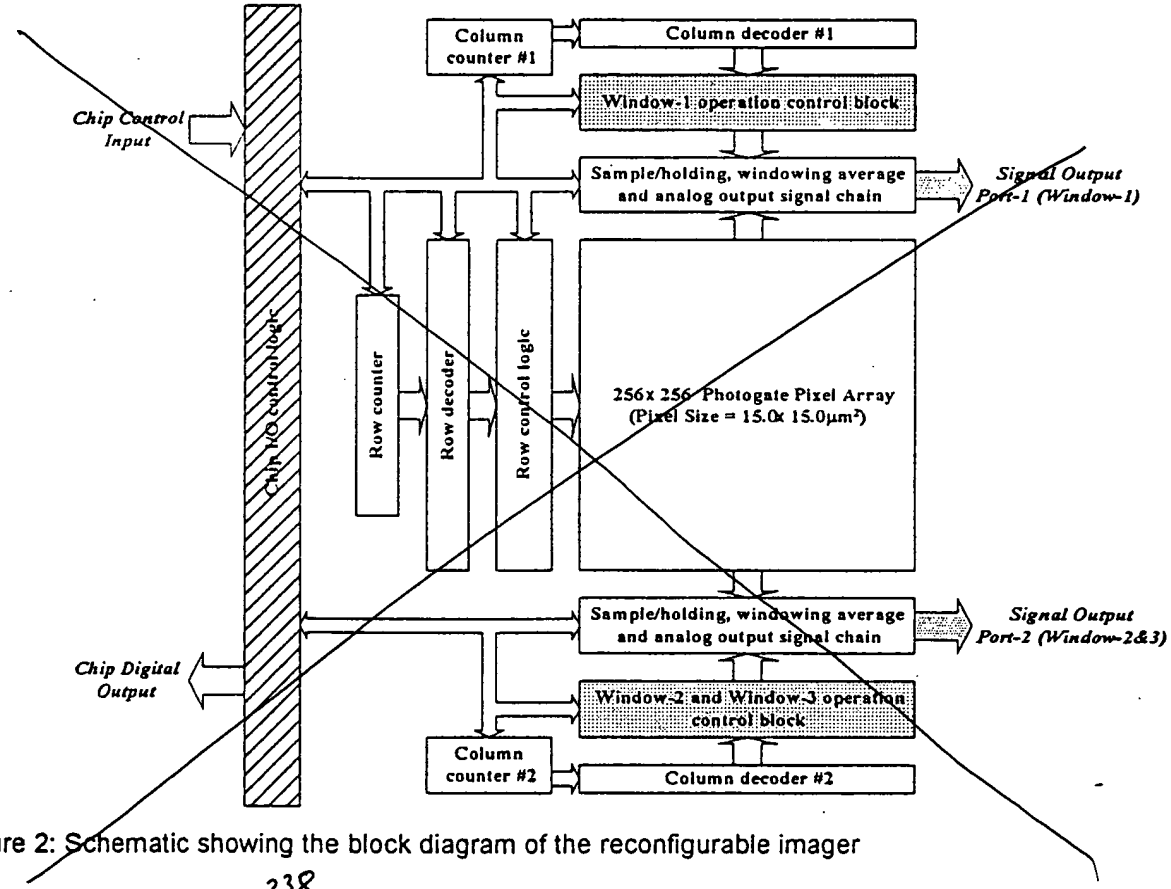


Figure 2: Schematic showing the block diagram of the reconfigurable imager

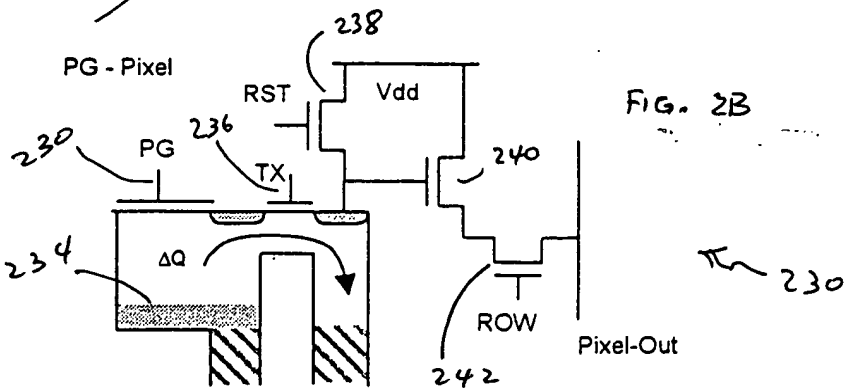


FIG. 2B

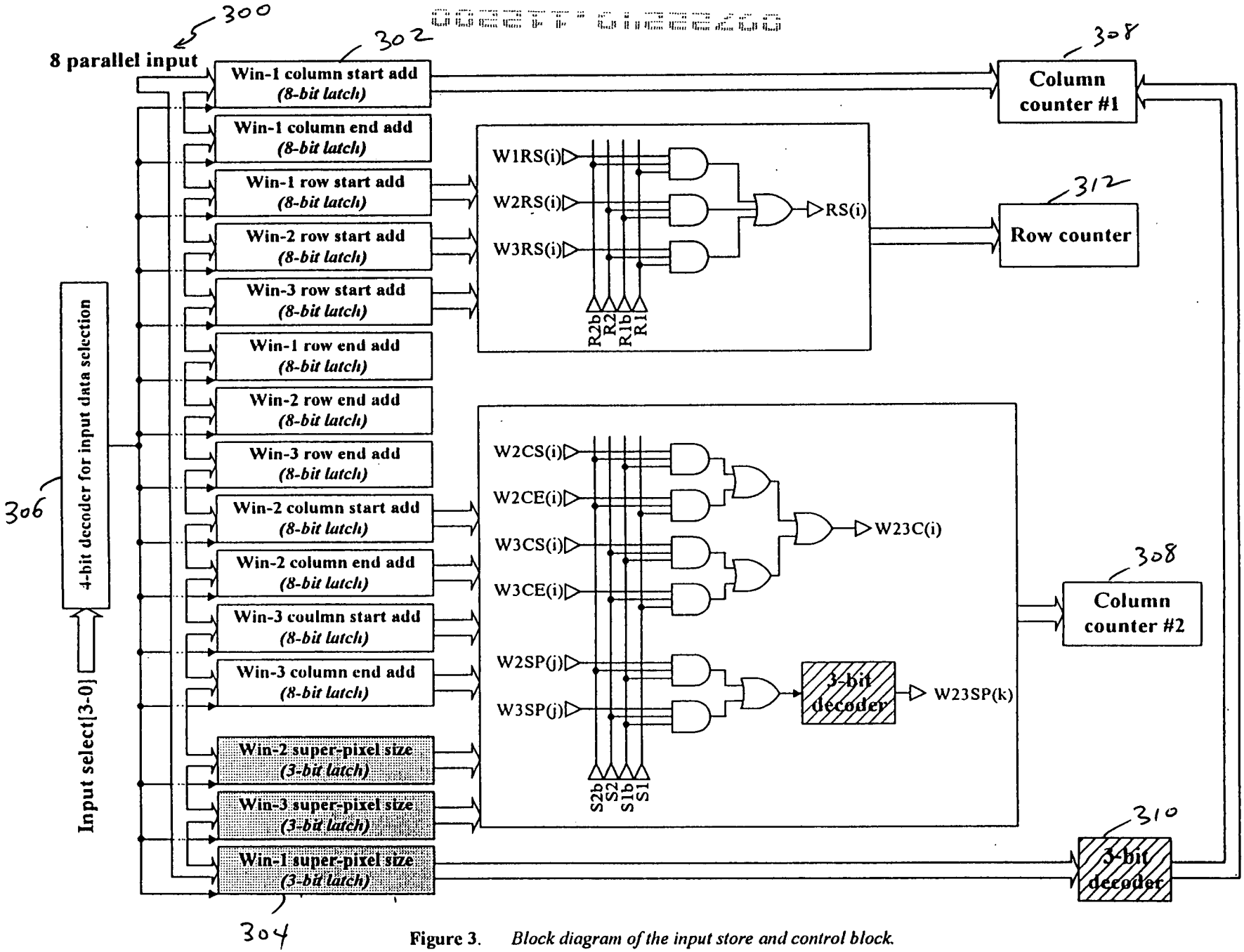
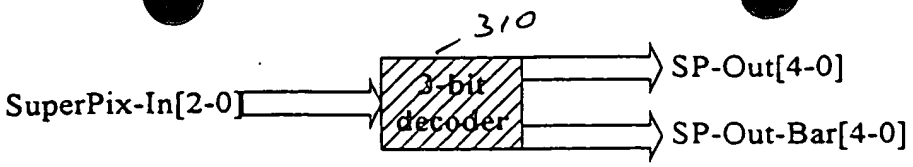


Figure 3. *Block diagram of the input store and control block.*



Superpixel size	In2	In1	In0	Out4	Out3	Out2	Out1	Out0
1x1	0	0	0	0	0	0	0	0
2x2	0	0	1	0	0	0	0	1
4x4	0	1	0	0	0	0	1	1
8x8	0	1	1	0	0	1	1	1
16x16	1	0	0	0	1	1	1	1
32x32	1	0	1	1	1	1	1	1

Figure 4. *3-bit decoder and its truth table.*

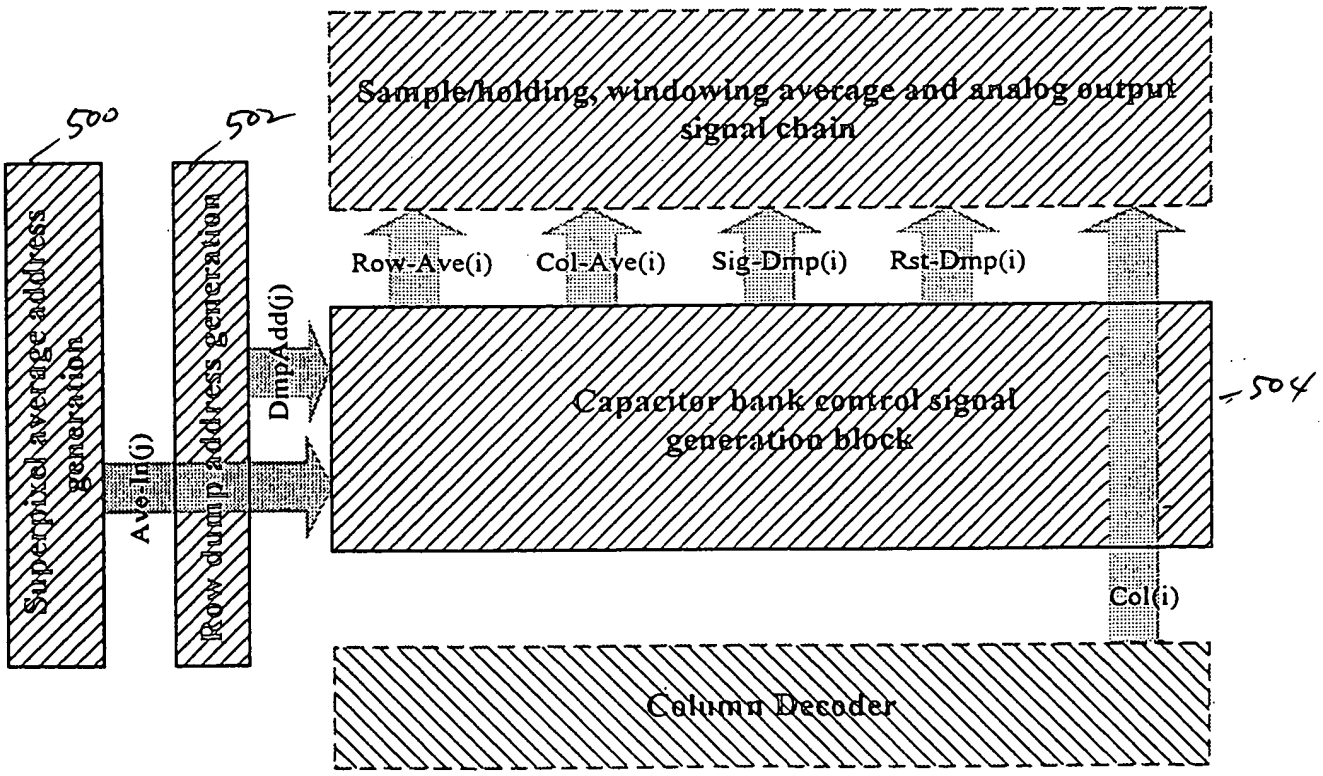


Figure 5. *Block diagram of window-1 operation control block.*

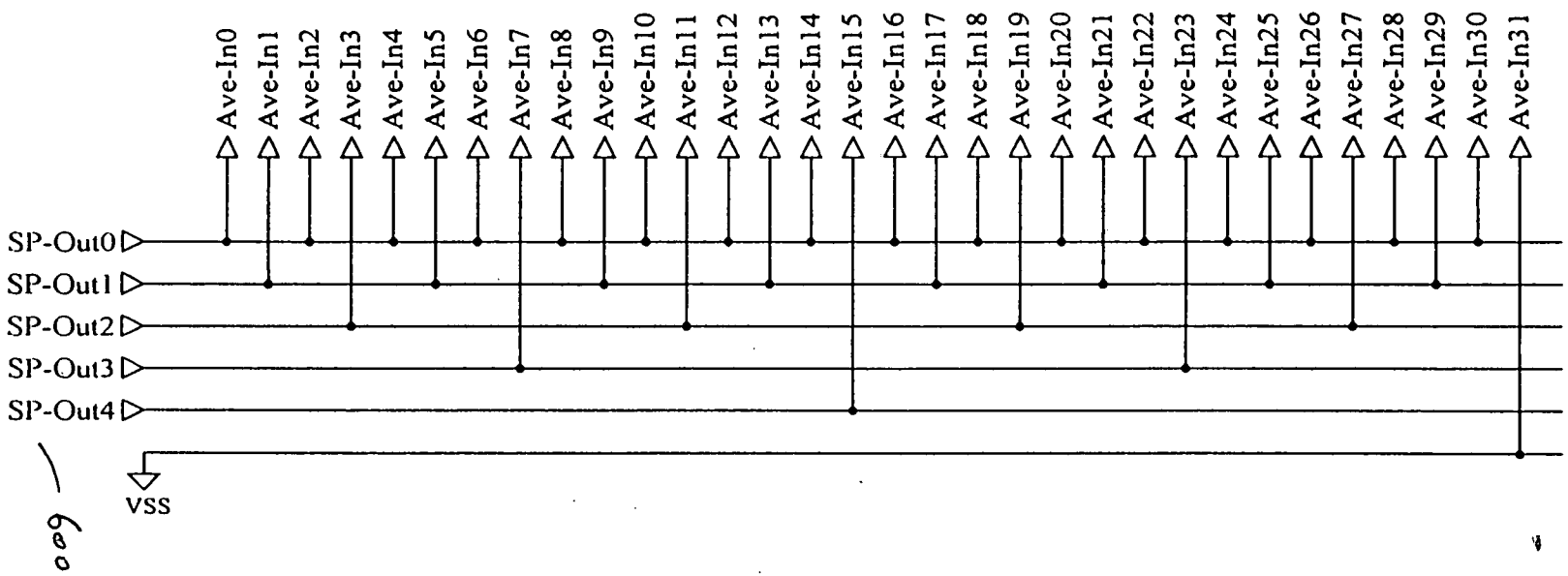


Figure 6. *Window-1 averaging address connection.*

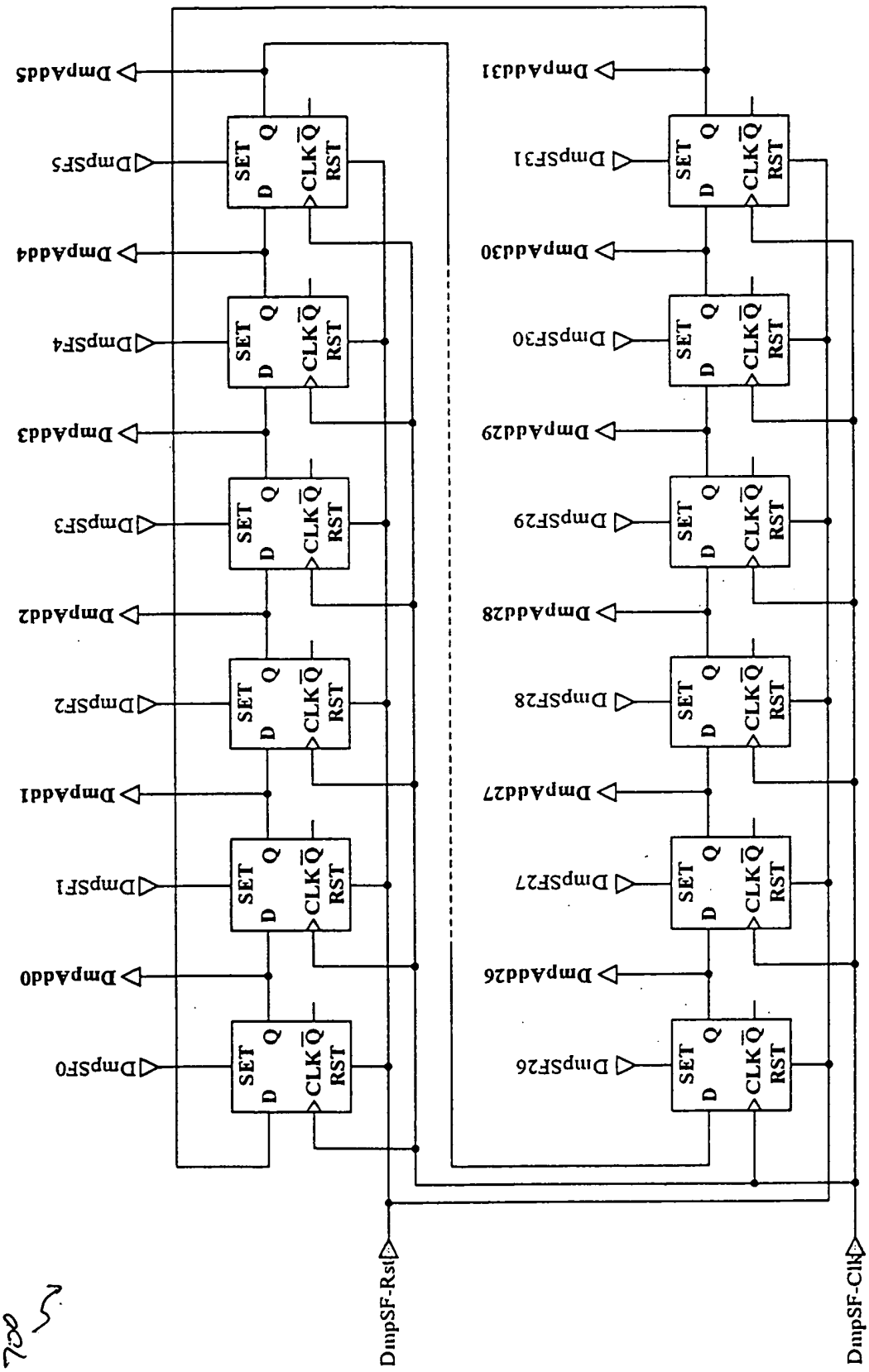


Figure 7. *32 shift registers of generating window-1 row dump addresses.*

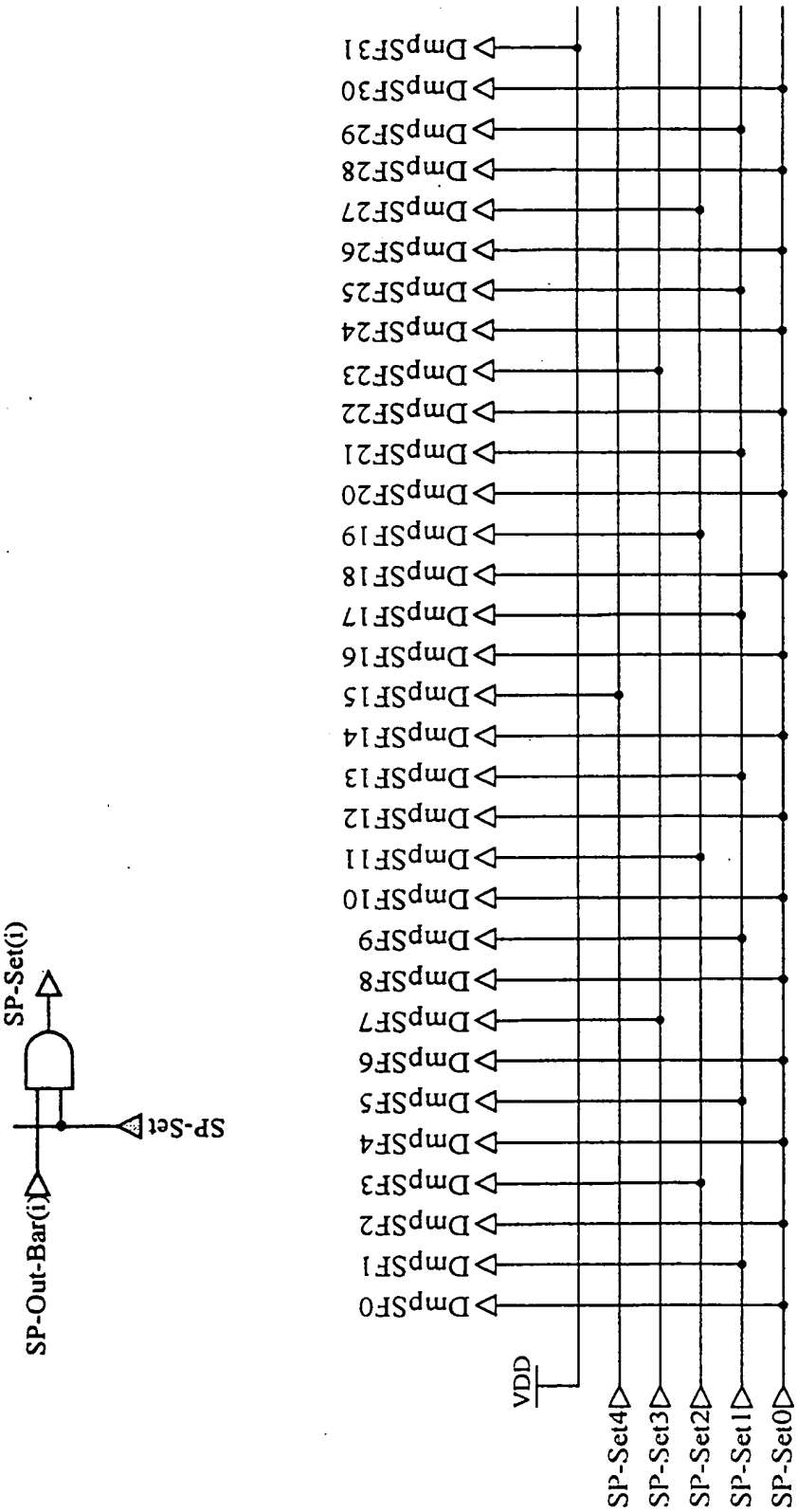


Figure 8. *Window-1 dumping address initial value generation.*

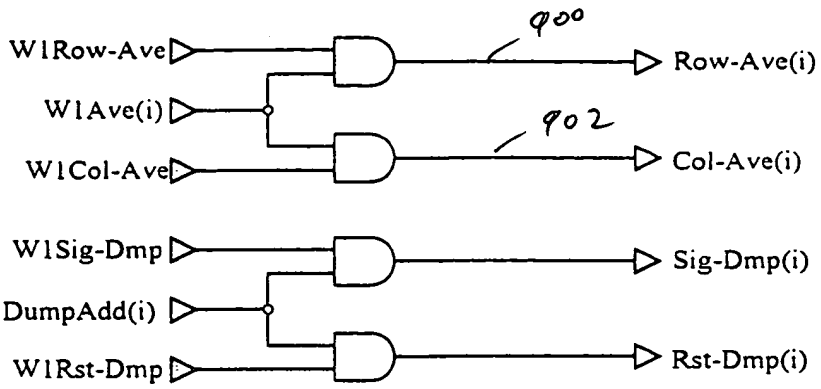


Figure 9. *Column circuit schematic of the capacitor bank control signal generation block*

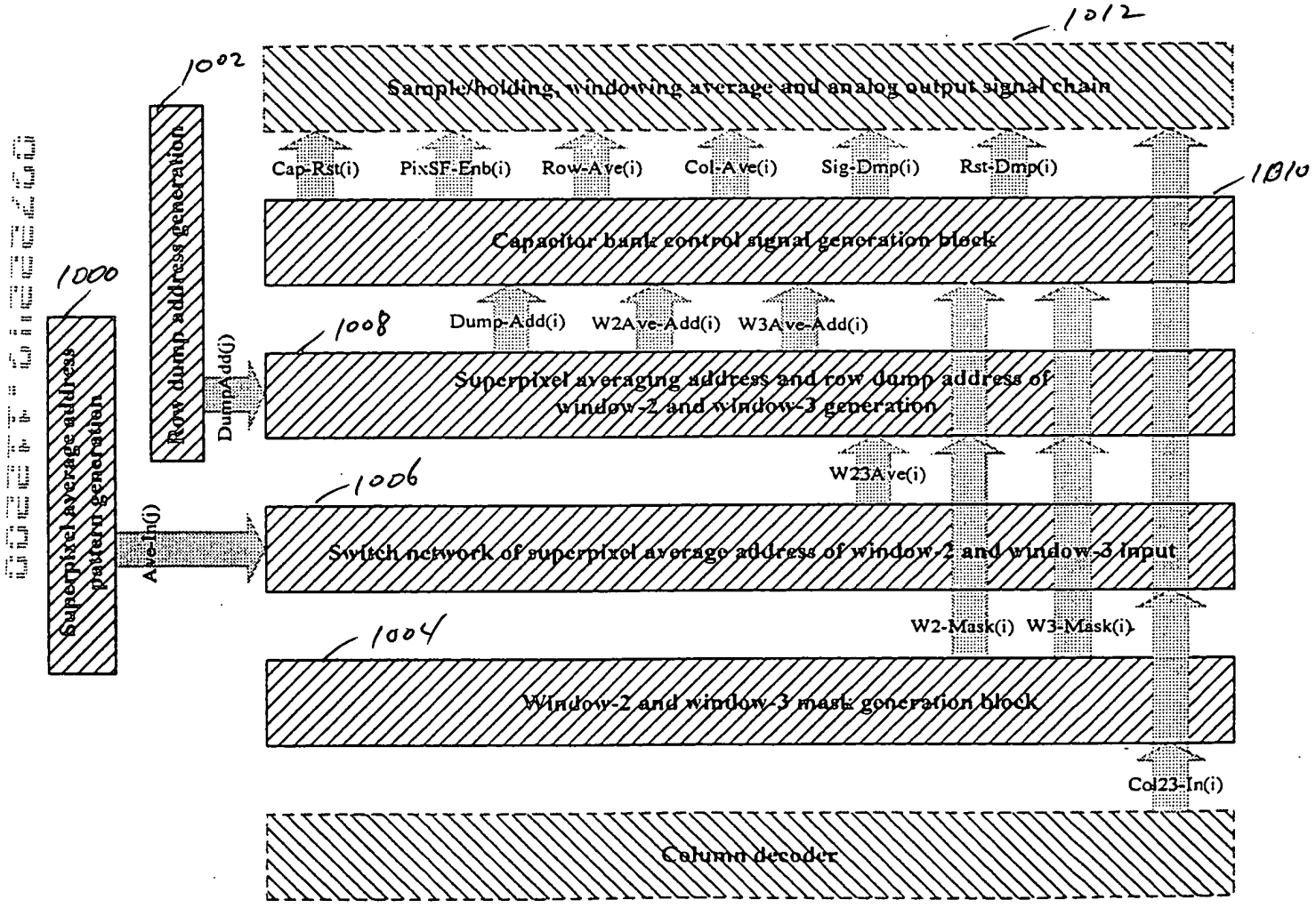


Figure 10. *Block diagram of window-2 and window-3 operation control block.*

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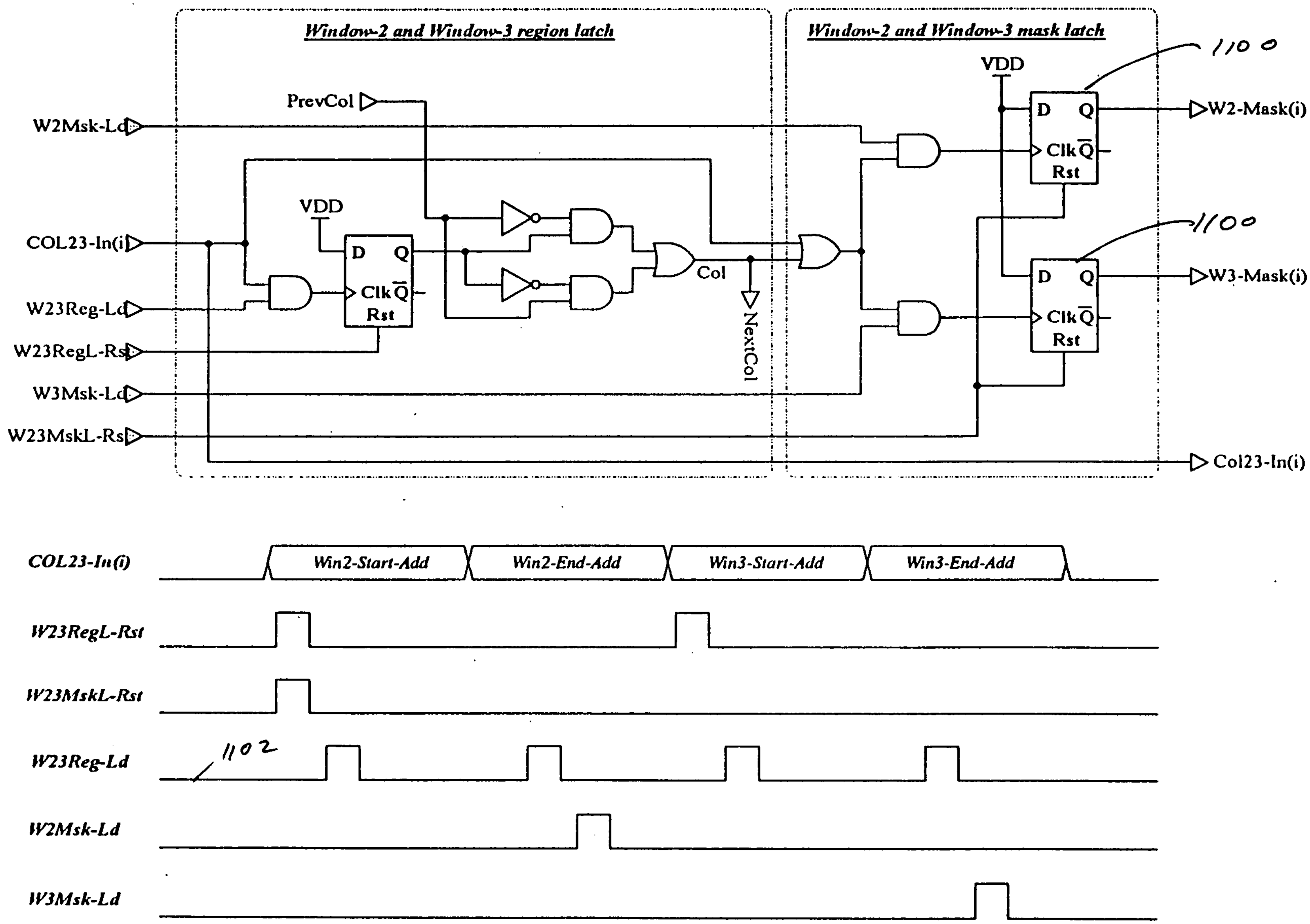

Figure 11. *Schematic and control waveform of window-2 and window-3 mask generation block.*

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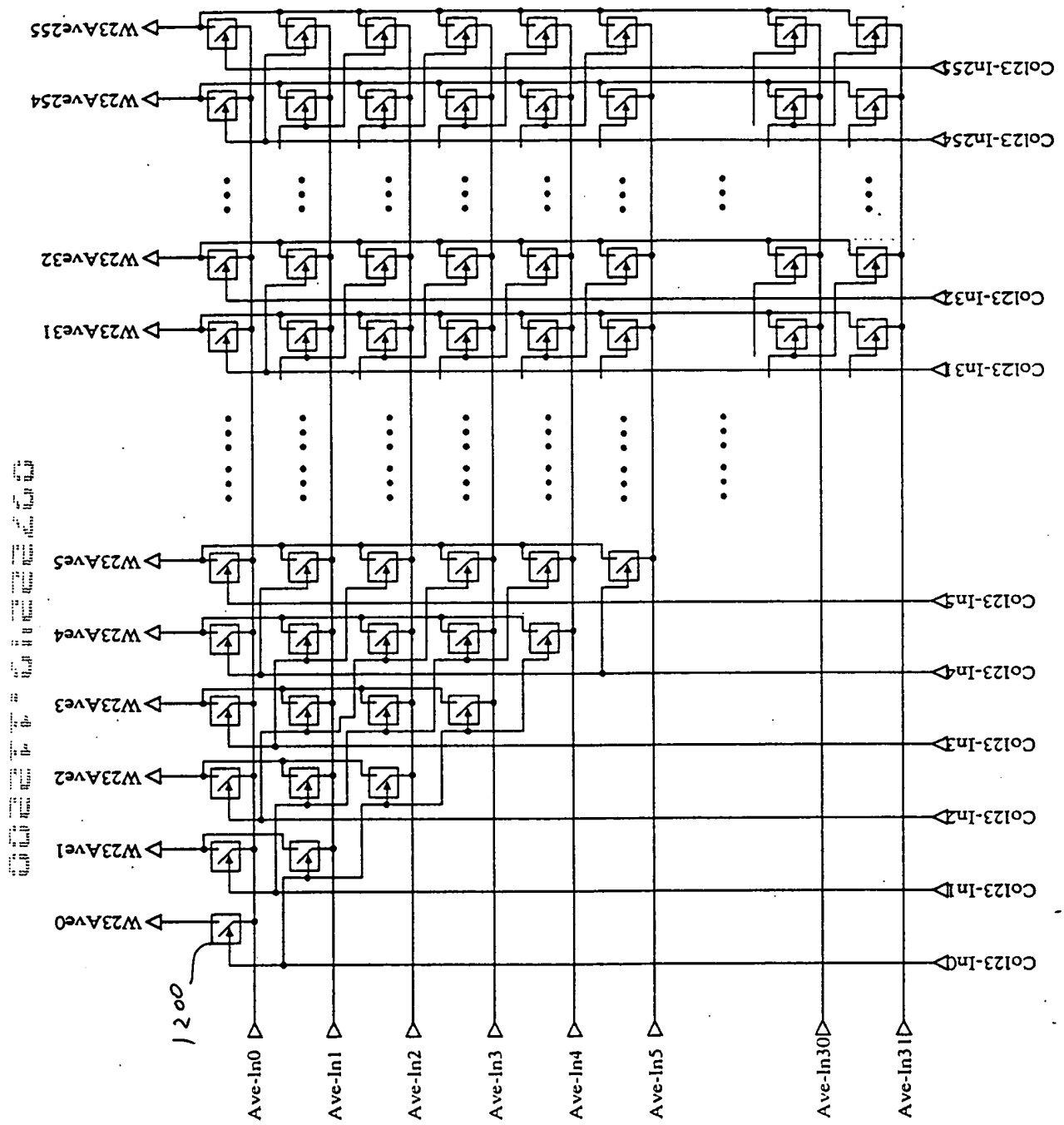

Figure 12. *Schematic of the switch network in window-2 and window-3 operation control block.*

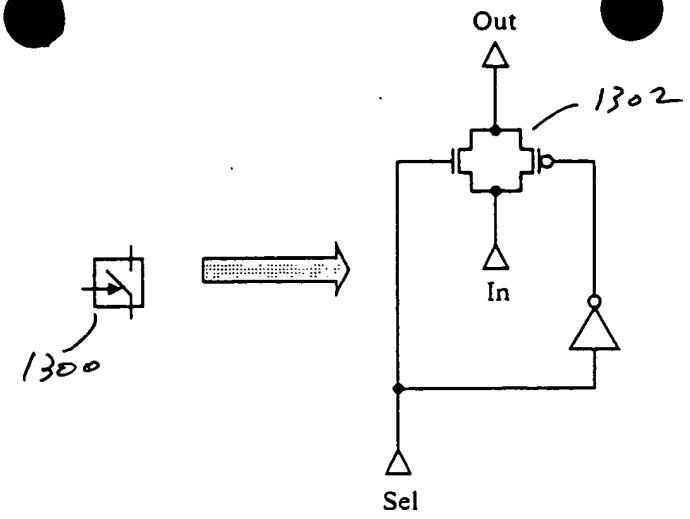

Figure 13. *Schematic transmission gate.*

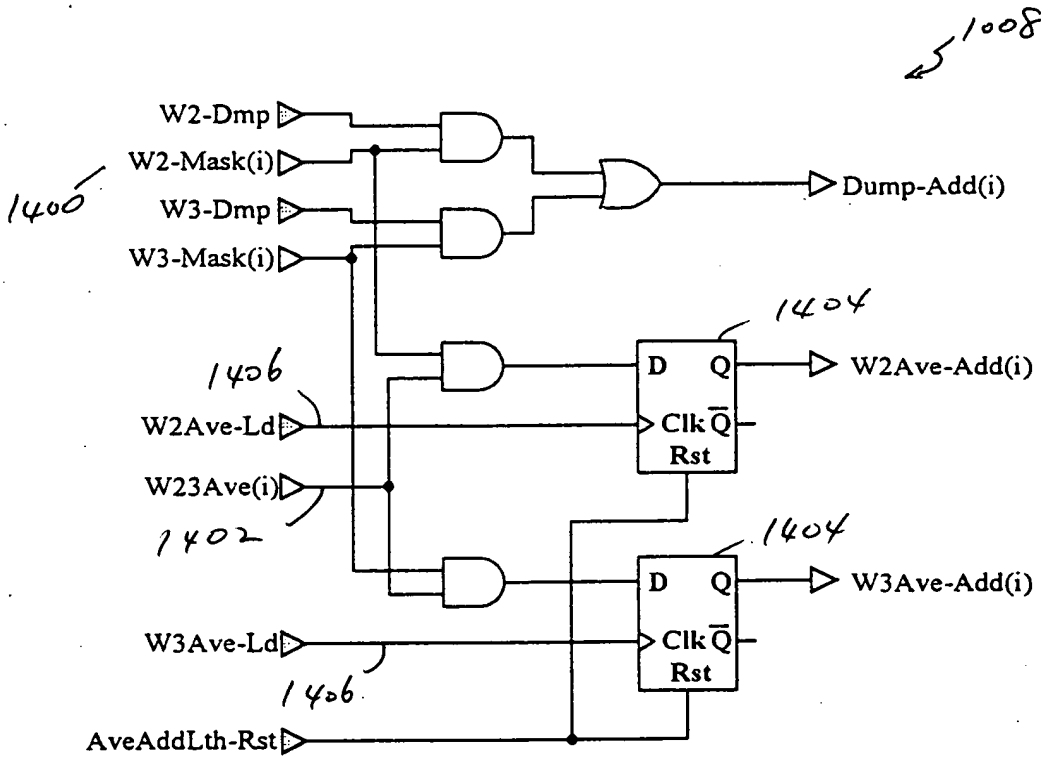

Figure 14. *Schematic of column circuit in superpixel averaging address and row dump address of window-2 and window-3 generation block*

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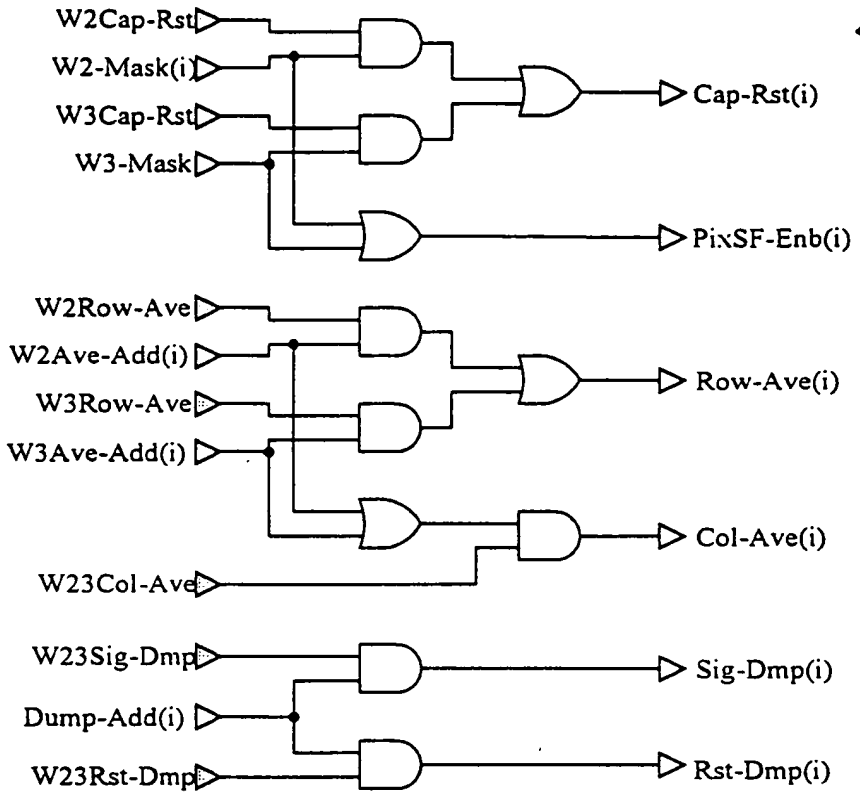


Figure 15. *Schematic of column circuit in the capacitor bank control signal generation block for window-2 and window-3.*

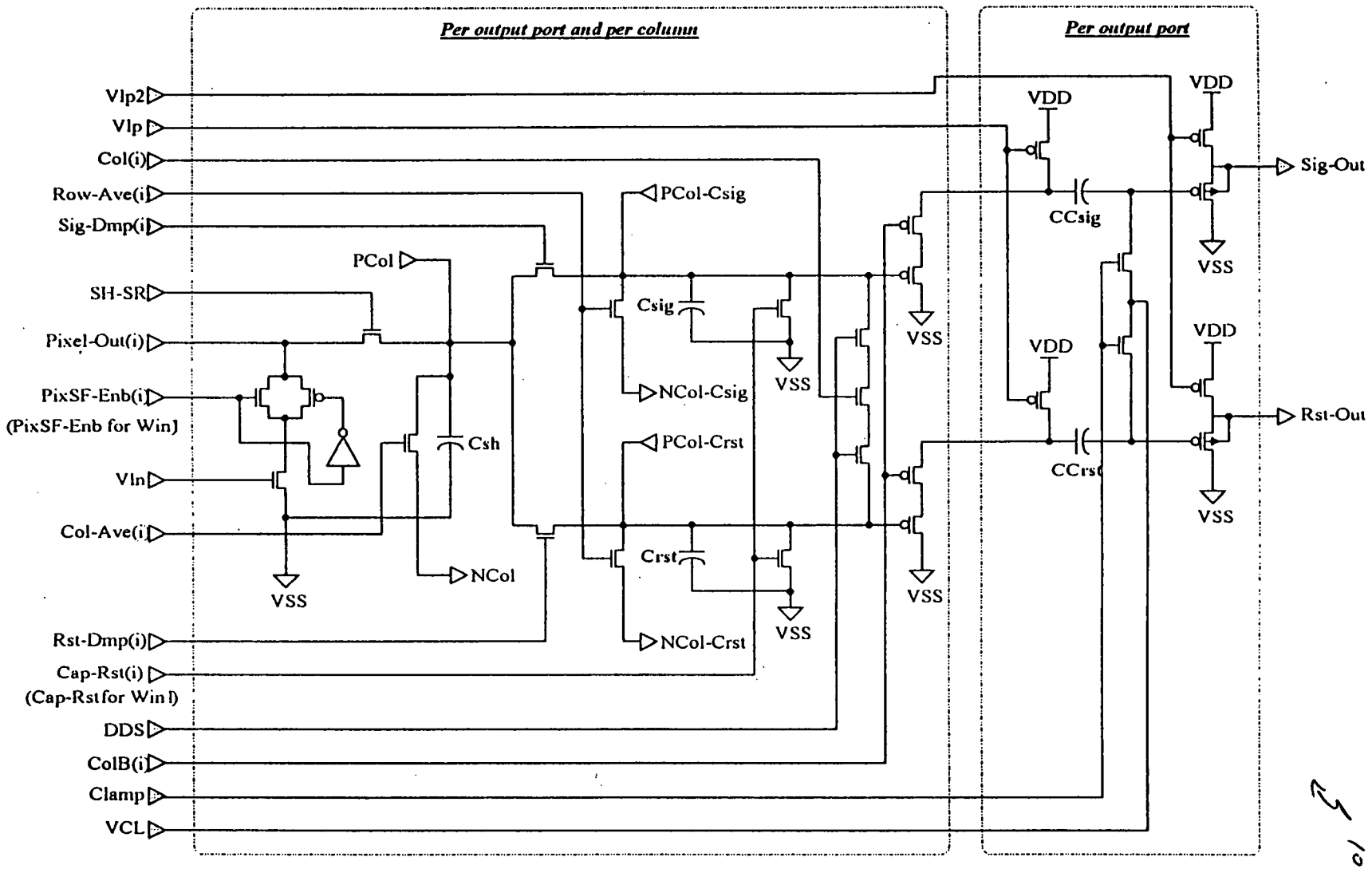


Figure 16. *Schematic of sample/holding, windowing average and analog output signal chain.*

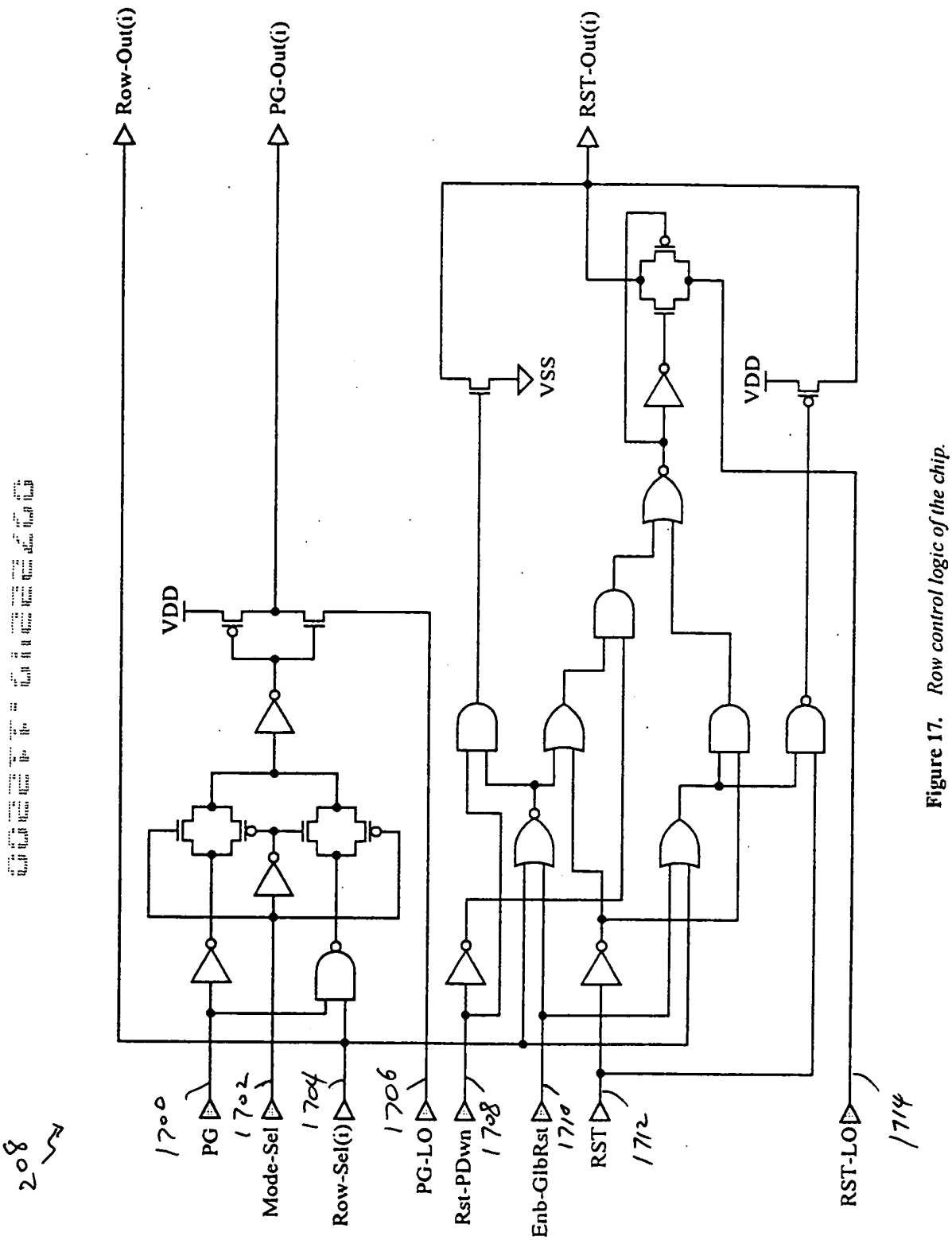


Figure 17. *Row control logic of the chip.*

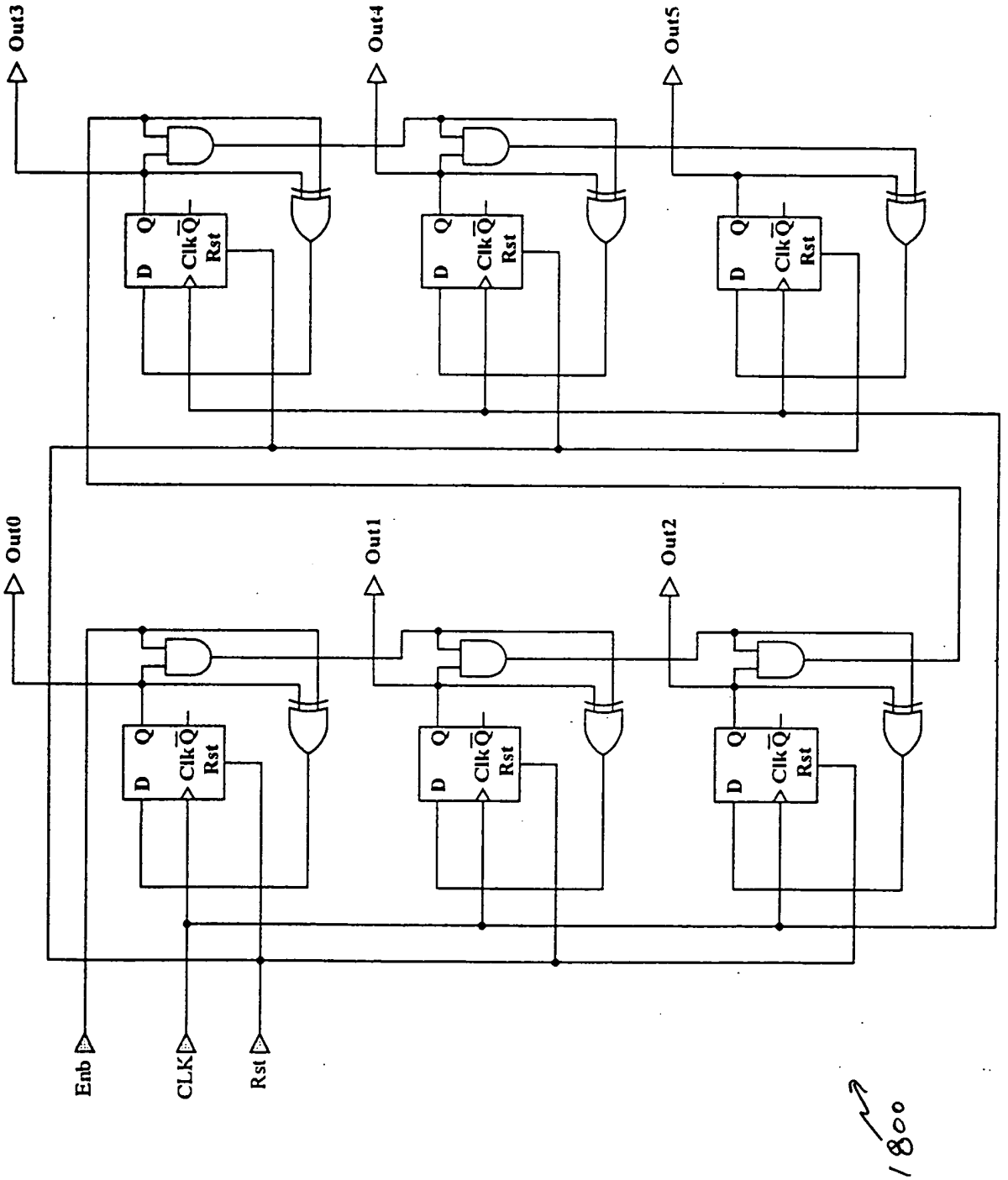


Figure 18. *Schematic of the 6-bit counter.*

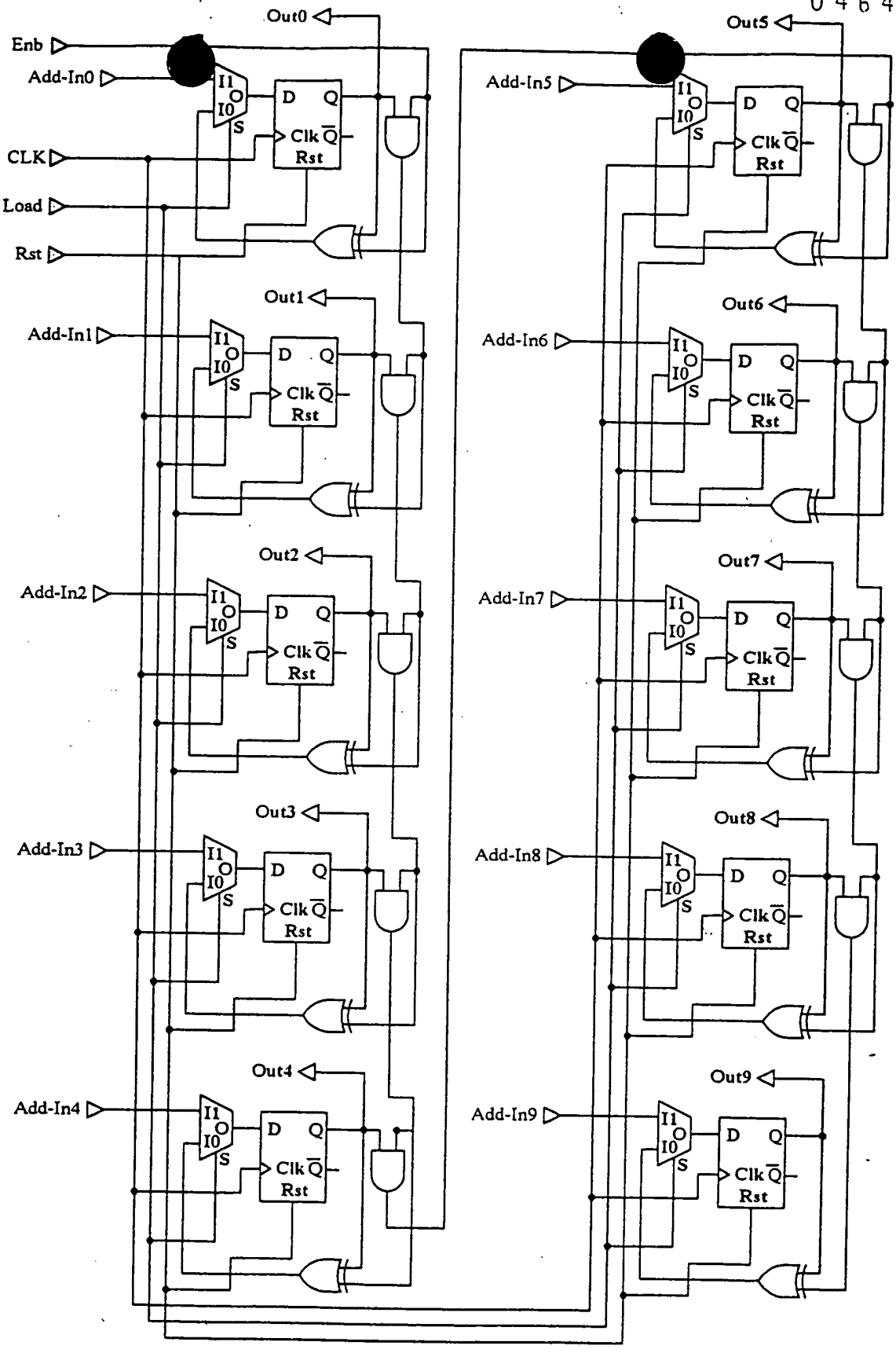


Figure 19. *Schematic of row counter.*

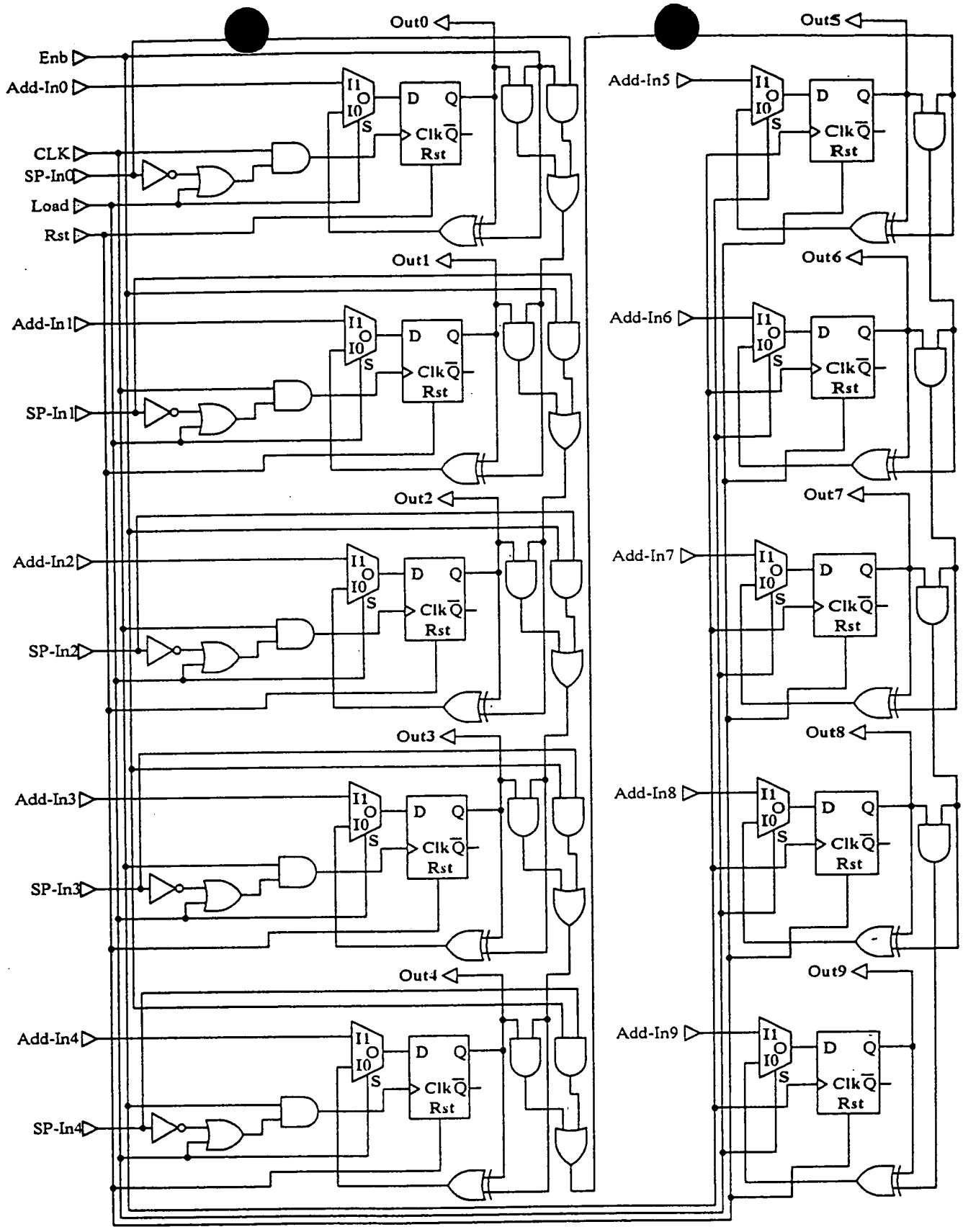


Figure 20. *Schematic of column counter.*

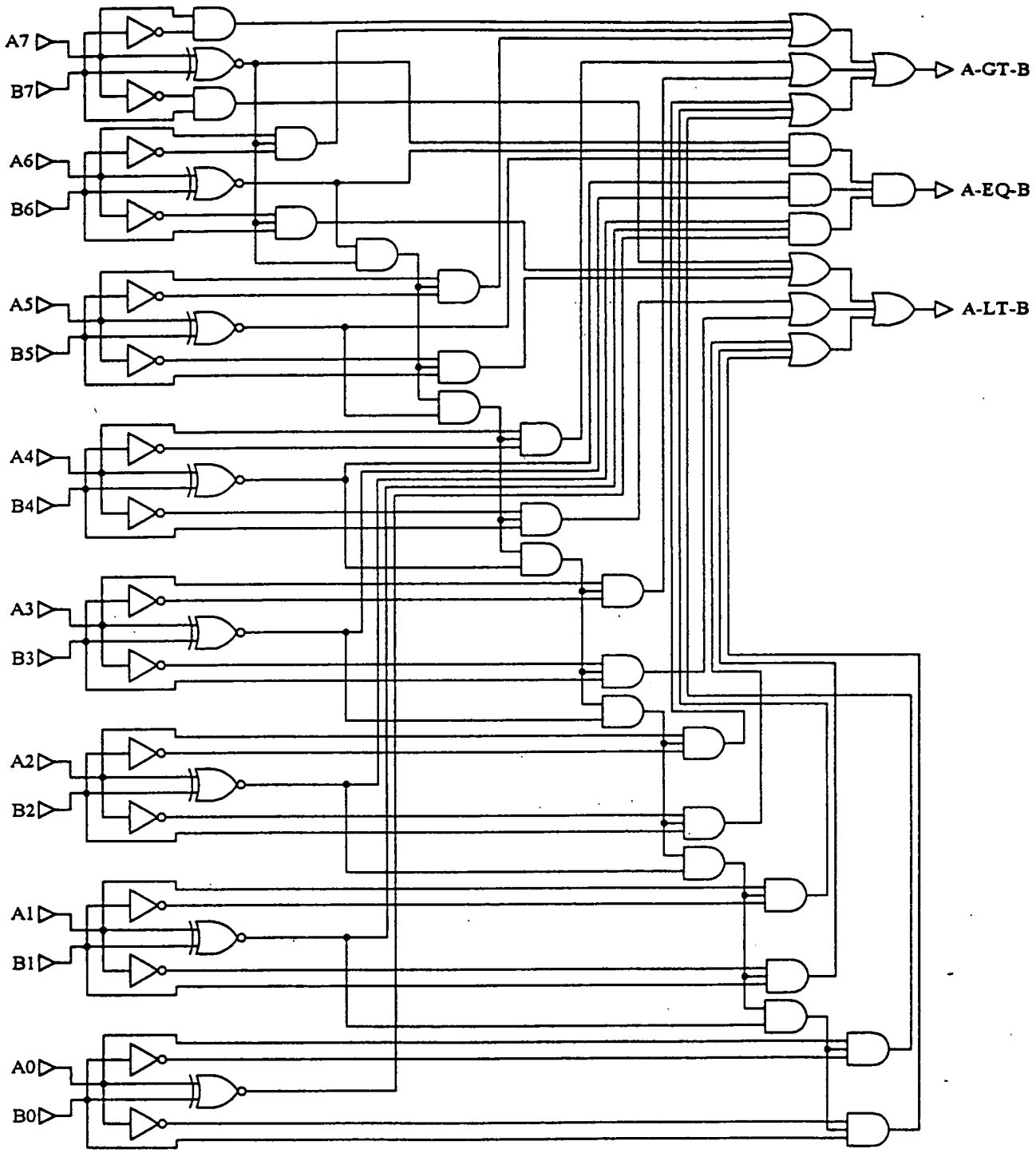


Figure 21. *Schematic of an 8-bit digital comparator.*

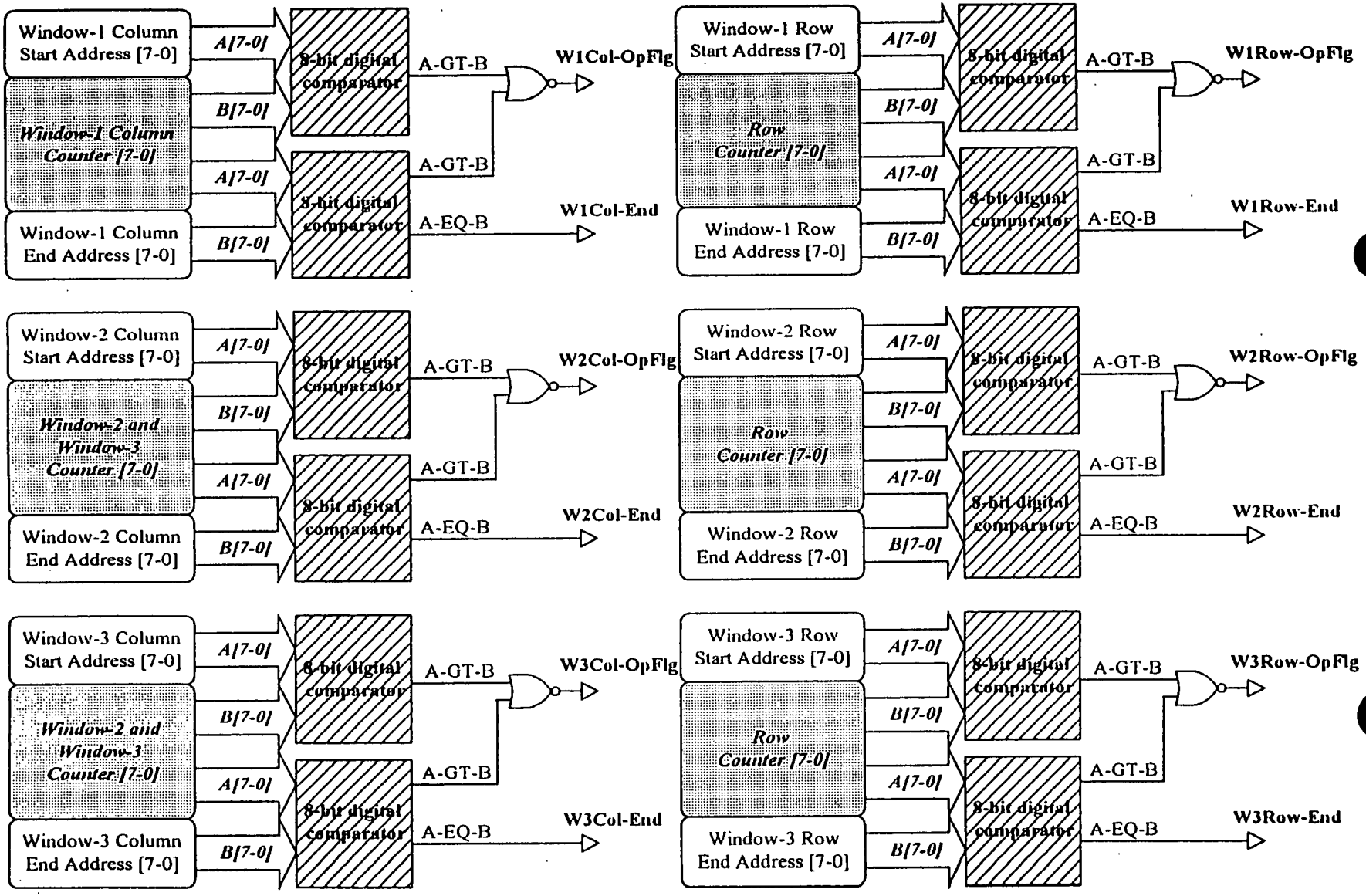


Figure 22. *Block diagram of generating row and column operation flags for the three windows.*

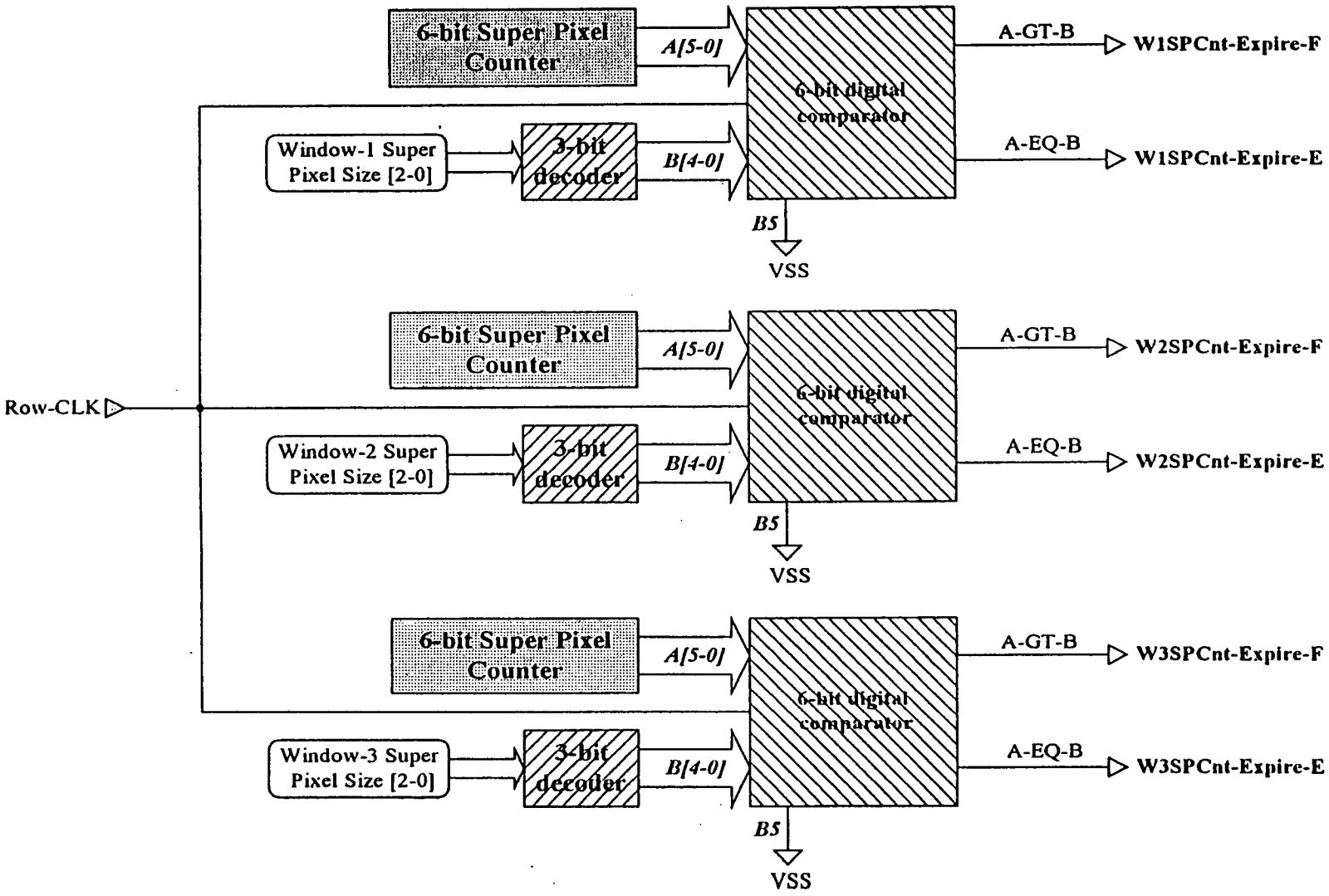
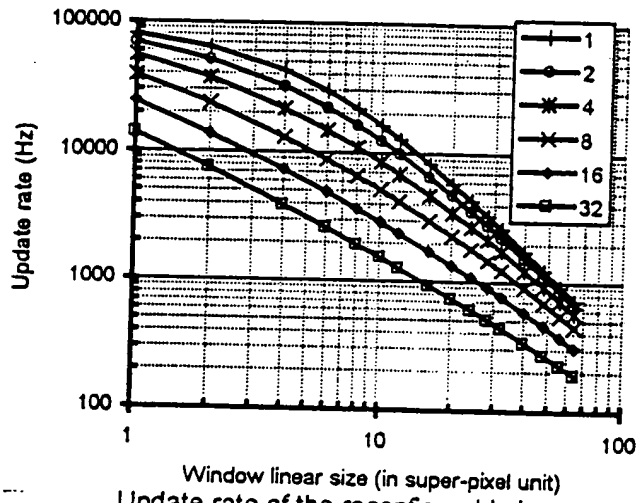
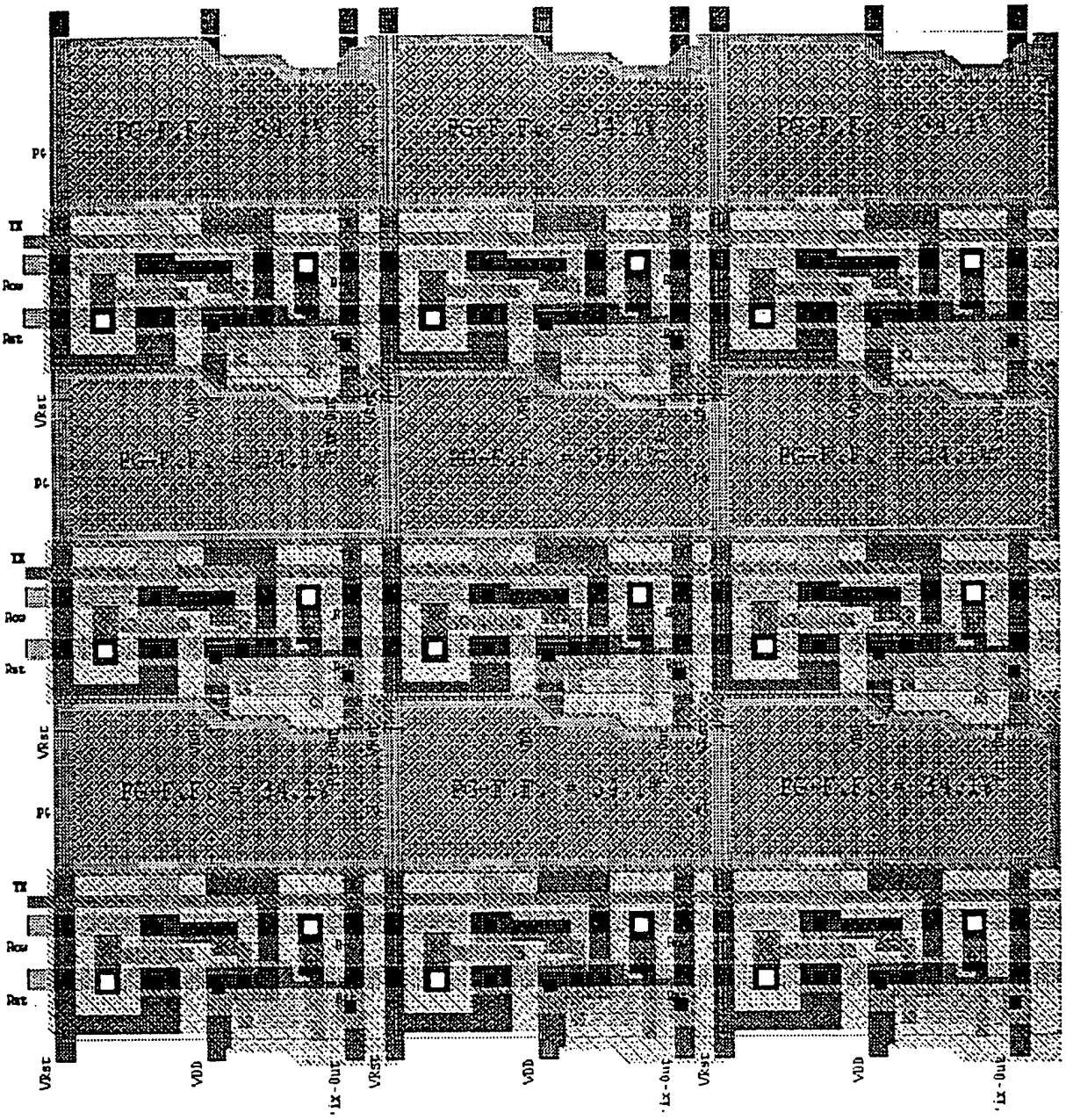


Figure 23. *Block diagram of generating superpixel expired flags for the three windows.*



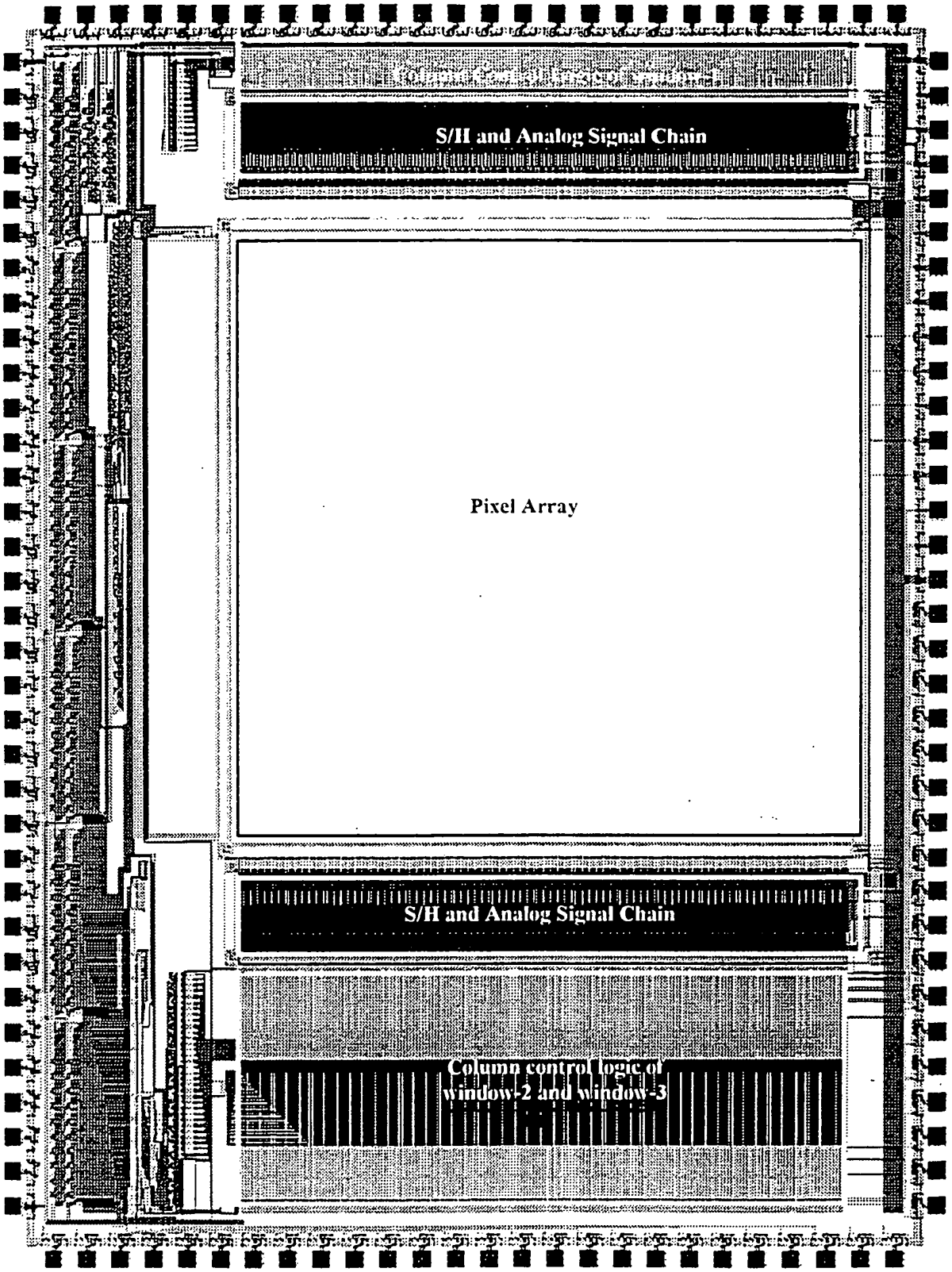
Update rate of the reconfigurable imager as a function of the super-pixel sizes

FIG. 24



Layout of 3x3 pixel array.

FIG. 25



Layout of the foveal vision chip.

FIG. 26

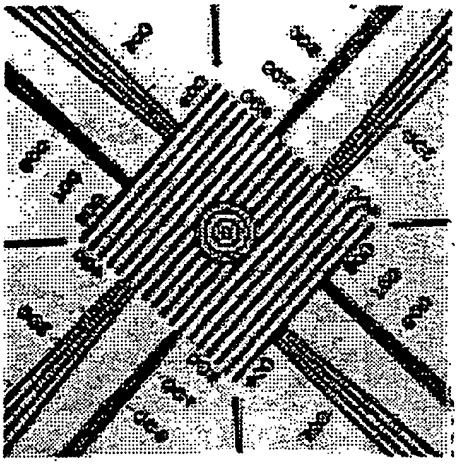


FIG. 27A: full-resolution image

FIG. 27B: block-averaged image

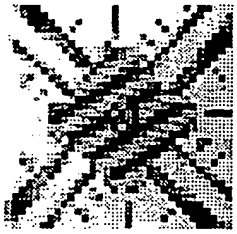


FIG. 27C: sub-sampled image

FIG. 27: Captured bar-pattern images from the reconfigurable imager at different resolutions

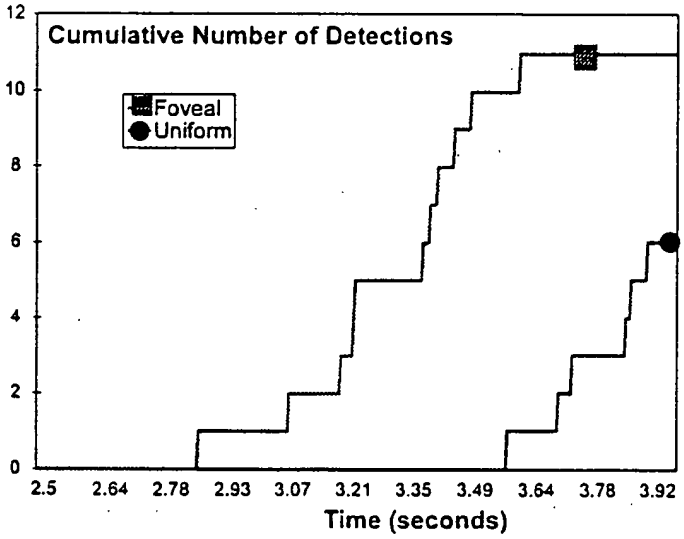


FIG. 28: Cumulative number of event detections and its speed for foveal and for uniform-acuity imagers

Table 1: Imager performance characteristics

Characteristics	Values
Imager format	256x256
Pixel Pitch	15 μm x 15 μm
Number of simultaneous ROIs	3
Max. Update rate	100 kHz
Super-pixel sizes	1x1, 2x2, 4x4, 8x8,16x16, 32x32
Power dissipation	< 10 mW
Noise	< 7 electrons
Dark current	100 pA/cm^2
Quantum Efficiency	22 %